SSC8033GS6A

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-30V	±20V	45mR@-10V	-4.5A
		62mR@-4V5	

➢ Description

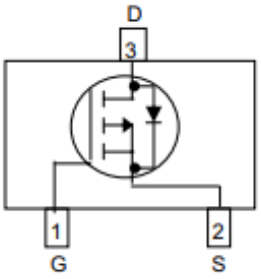
This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits and low in-line power loss are needed in a very small outline surface mount package.

➢ Applications

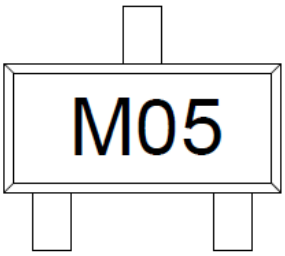
- TFT panel power switch
- High side DC/DC Converter
- High side driver for brushless DC motor
- Portable DVD, DPF

➢ Pin configuration

Top view



SOT23-3L



Marking

➢ Ordering Information

Device	Package	Shipping
SSC8033GS6A	SOT23-3	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-30	V
V_{GSS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current [a]	-4.5	A
I_{DM}	Pulsed Drain Current [b]	-16	A
P_D	Power Dissipation [c]	1.5	W
P_{DSM}	Power Dissipation [a]	0.85	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		150	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		85	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

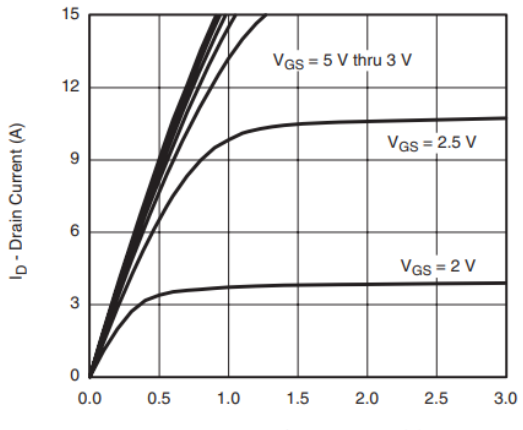
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

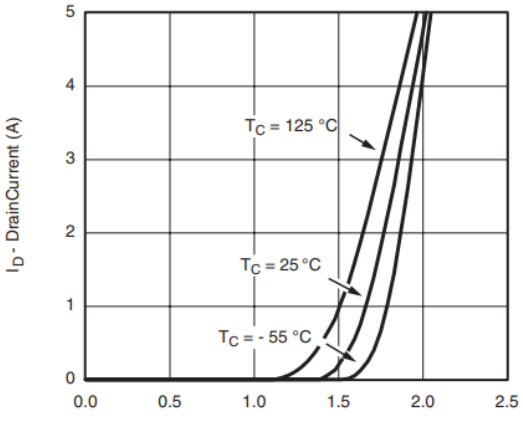
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=-250uA	-1	-1.5	-2	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-10V,ID=-4.1A		45	70	mR
		VGS=-4.5V,ID=-3A		62	90	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±20V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V,ID=-2.8A		6		S
V_{SD}	Forward Voltage	VGS=0V,IS=-0.75A		-0.8	-1.3	V
Ciss	Input Capacitance	VDS=-6V, VGS=0V, F=1MHZ		680		pF
Coss	Output Capacitance			72		
Crss	Reverse Transfer Capacitance			58		
$T_{D(ON)}$	Turn-on delay time	VGEN=-4.5V, VDS=-6V, RL=6R, RG=6R,ID=-1A		20		ns
Tr	Rise time			14		
$T_{D(OFF)}$	Turn-off delay time			65		
Tf	Fall time			21		

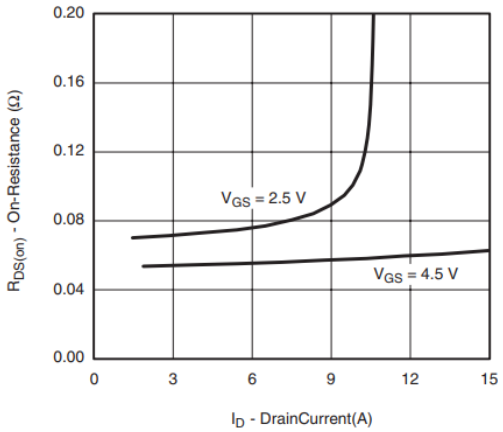
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



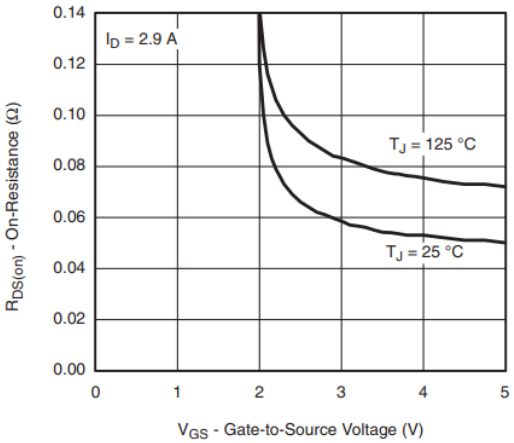
Output Characteristics



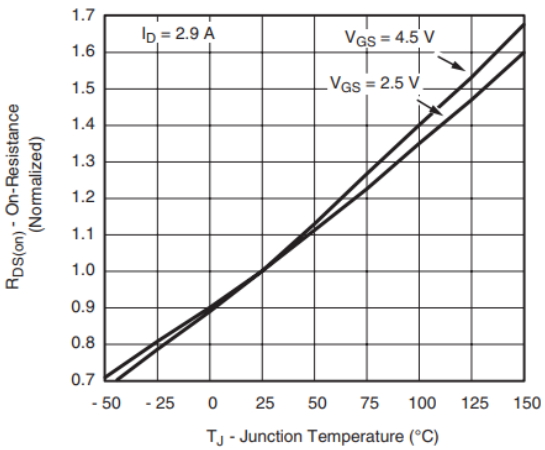
Transfer Characteristics



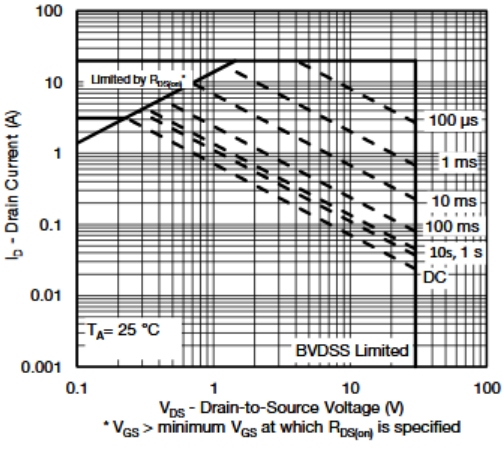
On-Resistance vs. Drain Current and Gate Voltage



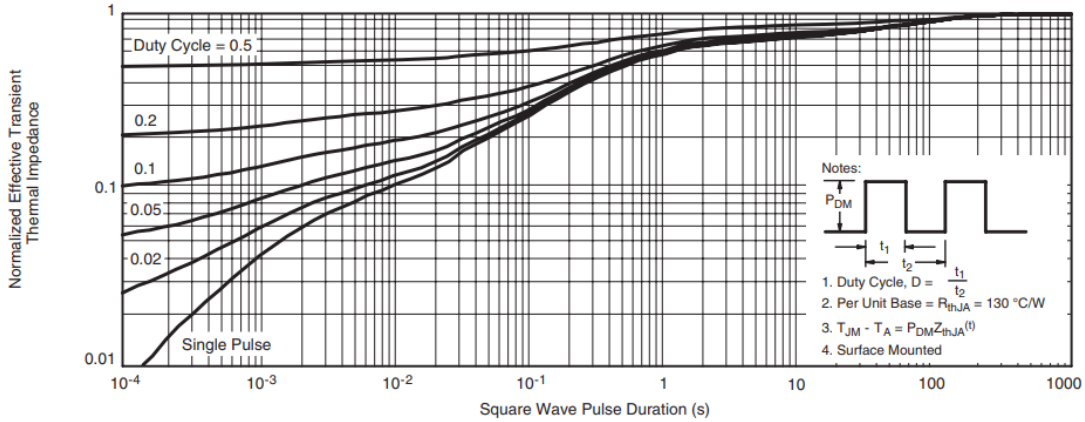
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

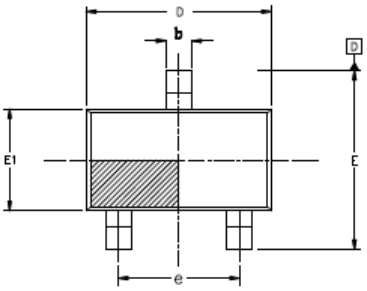


Safe Operating Area, Junction-to-Ambient

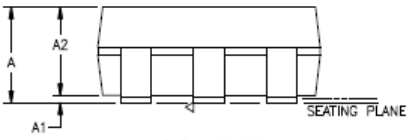


Normalized Thermal Transient Impedance, Junction-to-Ambient

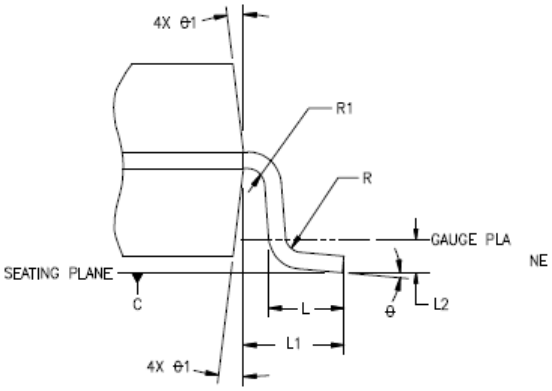
➢ Package Information

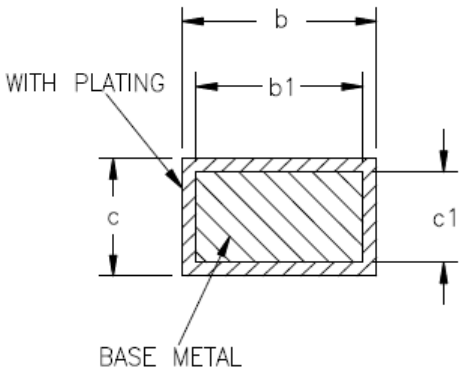


TOP VIEW



SIDE VIEW





SYMBOL	MIN	NOM	MAX
A	--	--	1.35
A1	0	--	0.15
A2	1.0	1.1	1.2
b	0.35	--	0.45
b1	0.32	--	0.38
c	0.14	--	0.20
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	1.8	1.9	2.0
L	0.35	0.45	0.6
L1	0.6REF		
L2	0.25REF		
R	0.1	--	--
R1	0.1	--	--
θ	0°	4°	8°
θ1	5°	10°	15°

NOTES:
1.All DIMENSIONS REFER TO JEDEC STANDARD MO-178
2.DIMENSION D DOES NOT INCLUDE MOLD FLASH
3.DIMENSION E1 DOSE NOT INCLUDE MOLD FLASH
4.FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.

SOT23-3L

➢ History Version

V1.0	Product datasheet	2018-06-01
V2.1	Update POD	2020-08-28

DISCLAIMER